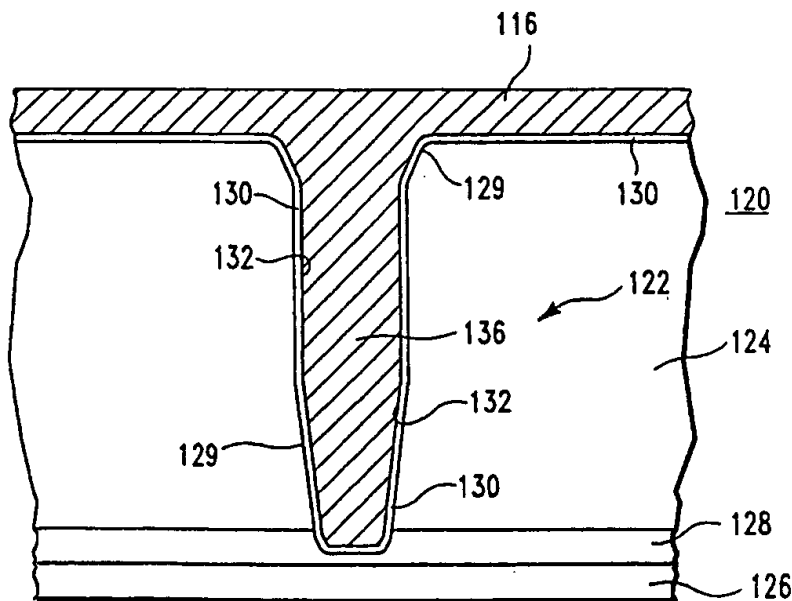




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<p>(54) Title: METHOD OF DEPOSITING A COPPER SEED LAYER WHICH PROMOTES IMPROVED FEATURE SURFACE COVERAGE</p>		
<p>(57) Abstract</p> <p>We have discovered a method of improving step coverage of a copper seed layer (132) deposited over a semiconductor feature surface (129) which is particularly useful for small size features having a high aspect ratio. Using a contact via (122) as an example of a high aspect ratio feature, we have demonstrated that despite previously-held views, it is possible to increase the copper seed layer coverage simultaneously at the bottom of the via and on the wall of the via by increasing the percentage of the depositing copper species which are ions. The percentage of species ionization which is necessary to obtain sufficient step coverage for the copper seed layer is a function of the aspect ratio of the feature. This increase in the percentage of copper species which are ionized can be achieved using techniques known in the art, such as, for example, laser ablation of the copper target, electron cyclotron resonance, hollow cathode, and applicants' preferred technique, an inductively coupled RF ion metal plasma. We have further discovered that when an inductively coupled plasma is used to increase ionization, an increase in power to the ionization source is not enough to obtain the desired percentage of ions in many cases. It is also necessary to increase the plasma gas pressure. Typically the plasma gas is argon, and the argon pressure in the copper seed layer deposition chamber is increased to fall within the range of about 20 to about 100 mT, preferably between about 30 mT and 70 mT.</p>		



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1 METHOD OF DEPOSITING A COPPER SEED LAYER WHICH
2 PROMOTES IMPROVED FEATURE SURFACE COVERAGE

3 **BACKGROUND OF THE INVENTION**

4 1. Field of the Invention

5 The present invention pertains to a method for depositing a copper seed layer
6 having improved step coverage over a feature surface, and to the improved feature
7 structure which is obtained using the method.

8 2. Brief Description of the Background Art

9 Due to the difficulty in etching a copper film to provide a desired semiconductor
10 interconnect pattern, one of the preferred methods of providing copper interconnects is
11 the damascene process, which requires the filling of embedded trenches and/or vias.

12 A typical damascene process for producing a multilevel structure having feature
13 sizes in the range of 0.5 micron (μ) or less would include: blanket deposition of a
14 dielectric material over a semiconductor surface; patterning of the dielectric material to
15 form openings; deposition of a conductive material over the surface of the dielectric
16 material in sufficient amount to fill the openings; and removal of excessive conductive
17 material from the substrate surface using a chemical reactant-based process, mechanical
18 method, or combined chemical-mechanical polishing techniques. Due to problems with
19 copper diffusion into underlying structures, a barrier layer is frequently used between the
20 dielectric material and the copper fill material. In addition, to improve the adhesion of the
21 copper fill to the barrier layer, a seed layer of copper is deposited over the barrier layer
22 prior to deposition of the bulk copper fill material.

23 A major problem encountered during the copper fill of a feature is the entrapment
24 of void spaces within the copper fill. For example, during copper fill of a feature such as
25 a trench or via using chemical vapor deposition (CVD) there is a tendency to create voids

1 within the filled opening; this is particularly true with regard to high aspect ratio features.
2 Other disadvantages of a CVD process are the contaminants from the CVD reactant
3 deposition source which may be found in the deposited conductive material and the costs
4 associated with use of this technology. Filling of the copper feature with evaporated or
5 sputtered copper is a cleaner process; however, the tendency to form voids still exists.
6 Further, evaporative deposition is a relatively slow process, decreasing production rates.
7 Sputtered copper may be used to provide copper fill, if used in combination with a reflow
8 of the copper. However, the reflow process is typically also a time consuming process.

9 A typical sputtering technique for filling of high aspect ratio features of less than
10 about 0.5 μm includes cold (typically below about 150 °C) deposition of sputtered
11 copper over the feature surface, followed by an annealing process (without deposition) at
12 temperatures in excess of about 400°C, to reflow the copper and obtain filling of the
13 trench or via. However, such a reflow process presently is limited to aspect ratios of
14 about 2:1 or less and typically requires more than a half hour of processing time.

15 U.S. Patent No. 5,246,885 to Braren et al., issued September 21, 1993, describes
16 the problems listed above, and proposes the use of a laser ablation system for the filling
17 of high aspect ratio features. Alloys, graded layers, and pure metals are deposited by
18 ablating targets comprising more than one material using a beam of energy to strike the
19 target at a particular angle. The ablated material is said to create a plasma composed
20 primarily of ions of the ablated material, where the plasma is translated with high
21 directionality toward a surface on which the material is to be deposited.

22 U.S. Patent No. 5,312,509 of Rudolph Eschbach, issued May 17, 1974, discloses
23 a manufacturing system for low temperature chemical vapor deposition of high purity
24 metals. In particular, a semiconductor substrate including etched patterns is plasma
25 cleaned; subsequently, the substrate is coated with adhesion and nucleation seed layers.
26 A reactor connected to the process chamber containing the substrate sublimates a precursor

1 of the metal to be deposited, which is then transported to the substrate. The heated chuck
2 on which the substrate sits heats the substrate above the dissociation temperature of the
3 precursor, releasing the metal from the precursor onto the substrate to nucleate the metal
4 species onto the seed layer on the substrate. Although an adhesion barrier layer and a
5 seed layer (if required) are said to be deposited using sputter deposition, the copper layer
6 is applied solely by CVD deposition, to avoid the sidewall voiding which is said to occur
7 if sputtering is used for the copper deposition.

8 U.S. Patent No. 5,354,712 to Ho et al., issued October 11, 1994, describes a
9 method for forming interconnect structures for integrated circuits. Preferably, a barrier
10 layer of a conductive material which forms a seed layer for metal deposition is provided
11 selectively on the side-walls and bottom of interconnect trenches defined in a dielectric
12 layer. Subsequently, a conformal layer of metal is selectively deposited on the barrier
13 layer within the interconnect trench.

14 Despite all of the above-described development efforts, there remained a need for
15 a method of producing copper interconnect features which did not require the use of
16 particularly complex equipment; which provided good step coverage for small, high
17 aspect ratio features; which could be carried out at temperatures below about 450 °C;
18 and, which produced an interconnect structure which is essentially void-free.

19 Very recently, copper filled semiconductor features were produced using
20 electroplating techniques employing particularly clean plating solutions. This method for
21 depositing copper works well when a continuous, conformal copper seed layer is in place
22 on the surface of the feature at the time of initiation of electroplating. However, if there
23 are any discontinuities in the copper seed layer, voids are created within the copper fill
24 where there are discontinuities in the seed layer. This makes it critically important to
25 have a continuous copper seed layer over the entire feature surface. When the feature
26 size is small (below 0.25 μm), and the aspect ratio is high (greater than about 3:1), for

1 example, obtaining a continuous seed layer of copper over the feature surface becomes
2 particularly difficult. Figure 1A shows a schematic of a cross-sectional view of a
3 copper-filled semiconductor contact via having a bottom diameter of $0.17\ \mu\text{m}$ and an
4 aspect ratio of about 7:1, where the step coverage of the copper seed layer is inadequate
5 and the copper fill contains numerous voids. To meet the challenge of filling features
6 having aspect ratios of greater than about 3:1, improvements in step coverage, especially
7 sidewall coverage are required.

8 SUMMARY OF THE INVENTION

9 We have discovered a method of improving step coverage of a copper seed layer
10 deposited over a semiconductor feature surface which is particularly useful for small size
11 features having a high aspect ratio. Using a contact via as an example of a high aspect
12 ratio feature, we have demonstrated that despite previously-held views, it is possible to
13 increase the copper seed layer coverage simultaneously at the bottom of the via and on
14 the wall of the via by increasing the percentage of the depositing copper species which
15 are ions. Further, the coverage can be optimized by adjusting the bias voltage of
16 (attractive forces on) the semiconductor substrate surface, as a function of the feature
17 dimensions.

18 The percentage of species ionization which is necessary to obtain sufficient step
19 coverage for the copper seed layer is a function of the aspect ratio of the feature.

20 Although the present invention contemplates the use of deposition species of which at
21 least 30 % are ions at the time they contact the substrate, for features having a $0.25\ \mu\text{m}$ or
22 smaller feature size, an aspect ratio of about 3:1 requires that about 50 % or more of the
23 copper species be ions at the time of deposition on the substrate. As the aspect ratio
24 increases to about 4:1, the percentage of species which are ions is preferably increased to
25 between about 60 % and 70 %. When the aspect ratio is about 5:1 or greater, the

1 percentage of species which are ions is preferably increased to greater than 80 %.
2 Although it is possible to approach 100 % of ionized species, typically the deposition rate
3 decrease makes operation under the required conditions impractical. As a result, for
4 many of the device features contemplated herein, the preferred percentage of ionization
5 ranges between about 50 % and about 90 %.

6 This increase in the percentage of copper species which are ionized can be
7 achieved using techniques known in the art, based on laser ablation of the copper target,
8 electron cyclotron resonance, hollow cathode, and applicants' preferred technique,
9 inductively coupled RF plasma. The use of an inductively coupled RF plasma is
10 described in detail herein.

11 We have discovered that when an inductively coupled plasma is used to increase
12 ionization, an increase in RF power to the ionization source is not enough to obtain the
13 desired percentage of ions in many cases. It is also necessary to increase the plasma gas
14 pressure. Typically the plasma gas is argon, although other inert gases such as krypton
15 and xenon can be used as well. In fact, the higher mass gases such as krypton or xenon
16 may be very effective in ionizing Cu atoms, although argon is preferred due to its
17 availability and lower cost. The plasma gas pressure in the copper seed layer deposition
18 chamber is increased to fall within the range of about 20 to about 100 mT, preferably
19 between about 30 mT and 70 mT, in order to achieve the desired percentage of ions in
20 the plasma.

21 BRIEF DESCRIPTION OF THE DRAWINGS

22 Figure 1A shows a schematic of a transmission electron microscope (TEM) cross-
23 sectional image of a copper-filled contact obtained using prior art methods for deposition
24 of the copper seed layer.

1 Figure 1B shows a schematic of a TEM cross-sectional image of a copper-filled
2 contact obtained using the method of the present invention for deposition of the copper
3 seed layer.

4 Figure 2A shows the bottom coverage obtained for a 0.25 μm diameter contact
5 via having an aspect ratio of about 5 : 1, as a function of the chamber pressure in the
6 copper deposition process chamber, when a lower level power is applied to the plasma
7 used to impact the sputtering target.

8 Figure 2B shows the sidewall coverage obtained for the 0.25 μm diameter contact
9 via shown in Figure 2A.

10 Figure 3A shows the bottom coverage obtained for a 0.25 μm diameter contact
11 via having an aspect ratio of about 5 : 1, as a function of the chamber pressure in the
12 copper deposition process chamber, when the power applied to the target sputtering
13 plasma is twice the power which was used for the Figure 2A contact via.

14 Figure 3B shows the sidewall coverage obtained for the 0.25 μm diameter contact
15 via shown in Figure 3A.

16 Figure 4A shows a simulated copper species ionization fraction as a function of
17 the pressure in the copper deposition process chamber. The simulation is based on
18 HPEM (Hybrid Plasma Equipment Model) Code available from Professor Mark
19 Kushner, University of Illinois.

20 Figure 4B shows the copper species ionization fraction as a function of the power

1 to an internal ionization coil which is positioned between the sputtering target and the
2 substrate support pedestal within the copper deposition process chamber.

3 Figure 5 is a schematic of a cross-sectional view of a sputtering chamber of the
4 kind which can be used to deposit a copper seed layer using the method of the present
5 invention. This illustration shows the critical elements of a high density plasma (ion-
6 deposition) sputtering chamber (or reactive-ion-deposition sputtering chamber). The
7 critical elements include a sputtering target to which DC power is applied, an RF
8 powered coil for creating and maintaining ionized species within a plasma over the
9 surface of the semiconductor substrate being processed, and a means for application of
10 RF power to the support pedestal on which the substrate sets, enabling the creation of an
11 enhanced bias on the substrate. When RF power is applied to the support pedestal, this
12 enables a more anisotropic direction of the ions toward the substrate and control over the
13 amount of force with which the ions strike the substrate.

14 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

15 The present invention pertains to a method of improving step coverage of a
16 copper seed layer deposited over a semiconductor feature surface, and is particularly
17 useful for small size features having a high aspect ratio. Improvement of the step
18 coverage refers to improvement of the ability to apply a continuous coating over a feature
19 surface despite feature topography. The method is based on the discovery that it is
20 possible to simultaneously increase the amount of bottom coverage and sidewall
21 coverage over a feature surface during the deposition of a given thickness of material
22 over the field surface of a semiconductor substrate. This simultaneous increase depends
23 on providing copper species at the surface of the substrate which contain at least a given
24 percentage of ions (the percentage required depends on the feature size and the aspect

1 ratio of the feature). Further, when using the apparatus of our preferred embodiments,
2 the percentage of species which are ions is increased by increasing the pressure in the
3 copper deposition process chamber.

4 1. DEFINITIONS

5 As a preface to the detailed description, it should be noted that, as used in this
6 specification and the appended claims, the singular forms "a", "an", and "the" include
7 plural referents, unless the context clearly dictates otherwise. Thus, for example, the
8 term "a semiconductor" includes a variety of different materials which are known to have
9 the behavioral characteristics of a semiconductor.

10 Specific terminology of particular importance to the description of the present
11 invention is defined below.

12 The term "aspect ratio" refers to, but is not limited to, the ratio of the height
13 dimension to the width dimension of a particular feature. When the feature has more
14 than one width dimension, the aspect ratio is typically calculated using the smallest width
15 dimension of the feature. For example, a contact via opening which typically extends in
16 a tubular form through multiple layers has a height and a diameter, and the aspect ratio
17 would be the height of the tubular divided by the diameter. The aspect ratio of a trench
18 would be the height of the trench divided by the minimal width of the trench, which
19 typically occurs at its base.

20 The term "bottom coverage" refers to, but is not limited to, the thickness of a
21 deposited material in the bottom of a feature as a fraction (or percentage) of the
22 deposition at the top (typically on the field surface) of the feature.

23 The term "completely filled" refers to the characteristic of the copper-filled
24 feature, wherein there is essentially no void space present in the copper-filled feature.

1 The term "copper" refers to copper and alloys thereof, wherein the copper content
2 of the alloy is at least 80 atomic %. The alloy may comprise more than two elemental
3 components.

4 The term "essentially void free feature" refers to, but is not limited to, a feature
5 which comprises a volumetric opening or space which is filled with a deposited material,
6 wherein the filled volume is essentially free of void spaces.

7 The term "feature" refers to, but is not limited to, contacts, vias, trenches, dual
8 damascene structures, and other structures which make up the topography of the
9 substrate surface.

10 The terms "ion-deposition sputtered", "ion metal plasma (IMP)", and "high
11 density plasma sputtered" refer to sputter deposition where the percentage of species
12 depositing on the substrate which are ionized is typically greater than about 50 %. There
13 are various methods for accomplishing ion-deposition sputtering, such as laser ablation
14 of the copper target, electron cyclotron resonance, hollow cathode, and our preferred
15 technique, inductively coupled RF plasma. The use of an inductively coupled RF plasma
16 is described in detail herein. Our inductively coupled plasma deposition preferably
17 employs magnetron sputter deposition (where a magnet array is placed behind the target).
18 A high density, inductively coupled RF plasma is created between the sputtering cathode
19 and the substrate support electrode (pedestal), whereby an increased portion of the
20 sputtered emission is in the form of ions at the time it reaches the substrate surface.

21 The terms "ion-deposition sputtered copper", "IMP copper", or "high density
22 plasma sputtered copper" refer to a copper deposition which was sputtered using the
23 techniques described above.

24 The terms "reactive ion-deposition", "reactive ion metal plasma (IMP)", or
25 "reactive high density plasma deposition" refer to sputtering of the kind described above,
26 wherein a reactive gas is supplied during the sputtering to react with the ionized material

1 being sputtered, producing an ion-deposition sputtered compound containing the reactive
2 gas element.

3 The term "sidewall coverage" refers to, but is not limited to, the thickness of
4 deposited material on the sidewall of the feature as a fraction (or percentage) of the
5 thickness at the top (typically on the field surface) of the feature.

6 The term "standard copper deposition" or "traditional sputtering" refers to a
7 method of forming a film layer on a substrate wherein a target is sputtered and the
8 material sputtered from the target passes between the target and the substrate to form a
9 film layer on the substrate, and no means is provided to ionize a substantial portion of the
10 material sputtered from the target before it reaches the substrate.

11 The term "TEM" refers to a transmission electron microscope.

12 II. AN APPARATUS FOR PRACTICING THE INVENTION

13 A process system which can be used to carry out the pre-cleaning step, the
14 deposition of barrier layers and the deposition of copper seed layers is the ENDURA®
15 Integrated Processing System available from Applied Materials, Inc. (Santa Clara,
16 California) The system is shown and described in United States Patents Nos. 5,186,718
17 and 5,236,868, the disclosures of which are incorporated by reference.

18 To further illustrate a typical apparatus which can be used to accomplish ion-
19 deposition sputter deposition from a desired target material, Figure 5 is a schematic of a
20 cross sectional view of the critical elements of an ion-deposition sputtering system.
21 Process chamber 500 may be used to deposit a copper seed layer using the method of the
22 present invention.

23 Process chamber 500 is typically a magnetron chamber which employs a standard
24 sputter magnet (not shown) to confine the sputtering plasma, enabling an increased
25 sputtering rate. In addition, the process chamber includes an inductively coupled RF

1 source 510 preferably located interior to the process chamber walls when the material
2 being sputtered is a metal. RF source 510 is typically in the form of a single, flat coil
3 508, positioned between a sputtering cathode (target) 502 and the substrate support
4 electrode 504, whereby a larger portion of the sputtered emission is in the form of ions at
5 the time it reaches the substrate surface. An RF power source 506 may be (optionally)
6 used to apply a bias to substrate support electrode 504, increasing the DC bias on
7 semiconductor substrate 505. Typically a shield 513 surrounds the area in which plasma
8 507 is created from gases which enter through channels 503. Shield 513 is surrounded
9 by a vacuum chamber 512 which enables the evacuation of gases from the substrate
10 processing area through evacuation channels (not shown). In the preferred embodiment
11 of the present invention, argon is typically the gas used to create sputtering ions which
12 impinge upon target 502 to produce depositing species such as copper species in the
13 present instance.

14 When it is desired to apply a fill layer of copper using an electroplating process,
15 this is preferably done in an electroplating bath of the kind known in the art, wherein the
16 reagents used in the electroplating process are of high purity. Such electrolytes are
17 available from Enthone-OMI having a sales office in Manhattan Beach, California.
18 Electroplating of copper is generally described in Ullmann's Encyclopedia of Industrial
19 Chemistry, Sixth Edition, 1998, and electroplating equipment which can be used for
20 copper plating of semiconductor surfaces is available from SEMITool® of Kalispell,
21 Montana. The electroplating may be done using DC only or DC-pulsed methods of
22 application.

23 It is preferred that the semiconductor structure not be exposed to air or moisture
24 after deposition of the barrier layer, until at least the seed layer of copper has been
25 applied over the barrier layer. It is preferred that the remainder of process steps are
26 completed through application of the copper fill via electroplating or other means while

1 the semiconductor structure is under a controlled ambient, to avoid the formation of
2 copper oxides and the corrosion of the copper in general within the interior of the feature.

3 4 III. THE METHOD OF THE INVENTION

5 Prior to the present invention, the theory was that deposition of a layer of copper
6 of a given thickness on the field surface of a semiconductor substrate provided a fixed
7 number of copper atoms available to cover the surface of a feature (such as a contact via)
8 residing within the substrate and open to the substrate surface. One could calculate the
9 amount of copper atoms deposited over the surface area of the opening and these would
10 be the atoms available to deposit over the feature surface underlying the opening. As a
11 result, by changing process parameters such that more of these copper atoms were
12 applied to the bottom of a contact or via, there would be less copper atoms available to
13 cover the sidewalls of the via. We have discovered that this is not the case. We have
14 discovered that it is possible to simultaneously increase the bottom coverage and
15 sidewall coverage of a contact via, provided a certain percentage of the copper species
16 applied to the substrate are ions. A possible explanation is that by increasing ionization
17 of the depositing metal, more of the copper species are attracted to the negatively biased
18 wafer and are able to penetrate deeper into higher aspect ratio features. Furthermore, the
19 increased ionization may decrease the sticking coefficient of depositing copper atoms to
20 less than one, leading to more scattering and redistribution of material from the bottom of
21 the feature to the sidewalls. The required percentage of ionization (or the ionized
22 fraction) of the copper species striking the substrate surface depends on the feature size
23 and the aspect ratio of the feature. For example, a contact via having a feature size of
24 about 0.25 μm or less and an aspect ratio of about 3: 1 requires that about 50 % or more
25 of the copper species be ions at the time of deposition on the substrate, to provide a
26 preferred, continuous sidewall coverage of the copper seed layer. As the aspect ratio

1 increases to about 4:1, the percentage of species which are ions is preferably increased to
2 between about 60 % and 70 %. When the aspect ratio is about 5:1 or greater, the
3 percentage of species which are ions is preferably increased to greater than 80 %.

4 Figure 1B shows a schematic of a TEM cross-sectional view of a semiconductor
5 structure 120 formed using the method of the present invention, which structure 120
6 includes a contact via 122 formed therein. The open surface 129 of a contact via 122 is
7 typically obtained by plasma etching of a layer of dielectric substrate 124 (typically
8 silicon dioxide). When the dielectric substrate 124 would be in contact with a copper fill
9 126, and the dielectric material (such as silicon oxide) is susceptible to diffusion by
10 copper, a barrier layer 130 is generally used between the copper and the dielectric
11 material. To provide improved adhesion of copper within the contact via 122, a copper
12 seed layer 132 is typically applied over barrier layer 130 prior to application of the bulk
13 of the copper fill material.

14 The preferred embodiments described herein are with reference to a substrate 126
15 which depends on the device functionality required. In the present instance, an etch stop
16 layer 128 of silicon nitride (other similar etch stop materials may be used) was deposited
17 over substrate 126, and a dielectric layer 124 of silicon oxide (other dielectric materials
18 may be used) was applied over the silicon nitride etch stop layer 128. A contact via
19 opening surface 129 having a feature size of about 0.17 μm and an aspect ratio ranging
20 from about 5 to about 7 was etched into silicon oxide layer 124. Subsequently, a barrier
21 layer 130 of tantalum nitride was applied over the interior surface of 129 of silicon oxide
22 using a reactive plasma vapor deposition technique of the kind known in the art. (It is
23 understood that should a dielectric material which is not subject to diffusion by copper be
24 used, such a barrier layer would not be necessary.) In the preferred embodiments
25 described herein, the tantalum nitride barrier layer was deposited using reactive ion-metal
26 plasma sputtering techniques of the kind described subsequently herein. However, other

1 deposition techniques such as CVD may be used as well. Typically the tantalum nitride
2 barrier layer 130 thickness ranged from about 150 to about 500 Å. We most commonly
3 used a barrier layer 130 thickness of about 250 Å. (It is understood that other, alternative
4 barrier layer materials such a tantalum, titanium, titanium nitride, tungsten, and tungsten
5 nitride may be used as well.)

6 Overlying barrier layer 130, a copper "seed" layer 132 was applied. And, finally,
7 a copper fill layer 136 was applied over copper seed layer 132. The purpose of the
8 copper seed layer 132 is to improve the adhesion of the copper fill 136 to barrier layer
9 130 and to provide the desired crystalline structure (preferably <111>) for transfer to
10 copper fill 136. The copper fill 136 may be applied using sputtering techniques under
11 specialized conditions, such as those described in co-pending U.S. patent application
12 Serial No. 08/855,059, filed May 13, 1997, titled: "Method of Sputtering Copper to Fill
13 Trenches and Vias". This patent application is assigned to the assignee of the present
14 invention and is hereby incorporated by reference in its entirety.

15 The copper fill may also be applied using techniques which provide a conformal
16 layer of copper, such as CVD, evaporation, or electroplating. In the present preferred
17 embodiments, electroplating was used to provide copper fill 136.

18 EXAMPLE ONE — COMPARITIVE EXAMPLE

19 Figure 1A illustrates the prior art, which is improved upon by the present
20 invention. Figure 1A shows a schematic of a TEM cross-sectional view of a
21 semiconductor structure 100 which includes a contact via 102 formed therein. The
22 feature size of contact via 102 was 0.17 μm, and the aspect ratio was about 7.

23 The open surface 109 of contact via 102 was obtained by plasma etching of a
24 layer of silicon oxide substrate 104 using techniques generally known in the art. A
25 barrier layer 110 of tantalum nitride was applied using ion metal plasma-deposition

1 sputtering conditions. In particular, the plasma source power was 1 kW DC; the RF
2 power to the ionization coil was 1.5 kW @ 2 MHz; the plasma gas flow was 50 sccm
3 argon and 20 sccm N₂; the process vessel pressure was 28 mT; the RF power applied to
4 the substrate support pedestal was 350 W @ 13.56 MHz, applied only during the latter
5 half of the deposition process.

6 Subsequently, a copper seed layer 112 was applied using the following process
7 conditions. Process chamber pressure was 20 mT; plasma source power was 2 kW DC;
8 the power to the ionization coil was 2 kW; the power applied to the substrate support
9 pedestal was 350 W during the latter half of the deposition process. The plasma source
10 gas was argon. The target composition was 100 % copper. The substrate temperature
11 during deposition was less than 100 °C; The substrate support pedestal temperature was
12 less than 50 °C.

13 These process conditions resulted in an ionized percentage of about 45 % of the
14 copper species striking the substrate surface. The bottom coverage was less than about
15 10 %, and sidewall coverage varied from about 0 % to about 10 %.

16 A copper fill layer 116 was applied over copper seed layer 112 using
17 electroplating techniques known in the art. Voids 114 were formed along the sidewalls
18 of contact via 102, leaving an incomplete fill of contact via 102 as shown in Figure 1A.

19 EXAMPLE TWO — A PREFERRED EMBODIMENT OF THE PRESENT 20 INVENTION.

21 Figure 1B illustrates a filled contact via prepared using the method of the present
22 invention. Figure 1B shows a schematic of a TEM cross-sectional view of a
23 semiconductor structure 120 which includes a contact via 122 formed therein. The
24 feature size of contact via 122 was 0.17 μ m, and the aspect ratio was about 7.

25 The preferred embodiments described herein were produced in a process chamber
26 capable of processing a 200 mm diameter silicon wafer. The open surface 129 of contact

1 via 122 was obtained by plasma etching of a layer of silicon oxide substrate 124 using
2 techniques generally known in the art. A barrier layer 130 of tantalum nitride was
3 applied using ion metal plasma-deposition sputtering conditions in the manner described
4 with reference to Figure 1A.

5 Subsequently, a copper seed layer 132 was applied using the following process
6 conditions. The process chamber pressure was 60 mT; the plasma source power was
7 1 kW DC; the ionization coil power was 2 kW @ 2 MHz; the RF bias power to the
8 substrate support pedestal was 350 W @ 13.56 MHz during the latter half of deposition.
9 The plasma source gas was argon. The target composition was 100 % copper. The
10 substrate temperature during deposition was less than about 100 °C; The substrate
11 support pedestal and the process chamber wall temperature was about 50°C. The
12 thickness of the copper seed layer on the field surface was about 200 nm.

13 These process conditions resulted in an ionized percentage of about 80 % of the
14 copper species striking the substrate surface. The bottom coverage was greater than
15 about 20 %, and sidewall coverage varied from about 5 % to about 10 %.

16 A copper fill layer 136 was applied over copper seed layer 132 using
17 electroplating techniques known in the art. No voids were formed within copper fill
18 layer 136 or along the sidewall areas of the via 122.

19 The enhanced step coverage achieved by the method of the present invention is
20 obtained as a result of the increased percentage of ions in the copper species contacting
21 the substrate surface, as previously described. The increase in the percentage of ions is
22 achieved in part due to use of the internal ionization coil 508 described with reference to
23 Figure 5. However, we discovered that due to the nature of copper atoms, it is necessary
24 to drastically increase the process chamber pressure during the deposition of copper, as
25 compared with process chamber pressures used for ion-deposition sputtering of other

1 materials (such as titanium, for example). It appears that the higher process chamber
2 pressures slow the progress of sputtered copper atoms through the area of the ionization
3 coil 508 due to increased collisions with argon atoms (used as the plasma source). This
4 permits more copper atoms to be ionized by the RF power supplied to ionization coil
5 508. The percentage of ionization can be increased by increasing the RF power itself,
6 but we have found that this alone is not generally adequate to obtain the desired
7 ionization percentage for copper species contacting the substrate. As previously
8 described, the process chamber pressure required is a function of the feature size and
9 aspect ratio. However, for feature sizes of about $0.25\ \mu\text{m}$ or less, having an aspect ratio
10 of about 4 or greater, it is typically necessary to use a process chamber pressure in excess
11 of 30 mTorr and preferably in excess of 50 mTorr. In the particular apparatus we used, a
12 process chamber pressure between about 40 mTorr and about 0.5 Torr is recommended,
13 with a preferred range being between about 40 mTorr and about 0.5 Torr, and a most
14 preferred range being between about 40 mTorr and about 100 mTorr.

15 Figure 2A shows a plot 200 of per cent bottom coverage (on vertical axis 202)
16 obtained for a copper seed layer deposited by the method of the invention (described with
17 reference to Figure 1) as a function of the process chamber pressure (on horizontal axis
18 204). Curve 206 represents data at the center of a semiconductor wafer substrate, while
19 curve 208 represents data at the edge of the semiconductor wafer substrate. The general
20 process conditions held constant were plasma source power at 1 kW DC; ionization coil
21 power at 2 kW RF (@ 2 MHz); no RF power to the substrate support platen; substrate
22 temperature was less than about $100\ ^\circ\text{C}$; process chamber wall temperature and substrate
23 support pedestal temperature were less than about $50\ ^\circ\text{C}$.

24 Figure 2B shows a plot 220 of minimum per cent sidewall coverage (on vertical
25 axis 222) obtained for a copper seed layer deposited by the method of the invention
26 (described with reference to Figure 1) as a function of the process chamber pressure (on

1 horizontal axis 224). Curve 226 represents data at the center of a semiconductor wafer
2 substrate, while curve 228 represents data at the edge of the semiconductor wafer
3 substrate. The general process conditions held constant were the same as described with
4 reference to Figure 2A.

5 The unexpected results illustrated by Figure 2A in combination with Figure 2B is
6 that it is possible to simultaneously increase both bottom coverage and sidewall coverage
7 of the interior of a contact via surface while depositing copper species by increasing the
8 pressure in the process chamber.

9 Figure 3A shows a plot 300 of per cent bottom coverage (on vertical axis 302)
10 obtained for a copper seed layer deposited by the method of the invention (described with
11 reference to Figure 1) as a function of the process chamber pressure (on horizontal axis
12 304). Curve 306 represents data at the center of a semiconductor wafer substrate, while
13 curve 308 represents data at the edge of the semiconductor wafer substrate. The general
14 process conditions held constant were plasma source power at 2 kW DC; ionization coil
15 power at 2 kW RF (@ 2 MHz); no RF power to the substrate support platen; substrate
16 temperature was less than about 100 °C; process chamber wall temperature and
17 substrate support pedestal temperatures were less than about 50 °C.

18 Figure 3B shows a plot 320 of minimum per cent sidewall coverage (on vertical
19 axis 322) obtained for a copper seed layer deposited by the method of the invention
20 (described with reference to Figure 1) as a function of the process chamber pressure (on
21 horizontal axis 324). Curve 326 represents data at the center of a semiconductor wafer
22 substrate, while curve 328 represents data at the edge of the semiconductor wafer
23 substrate. The general process conditions held constant were the same as described with
24 reference to Figure 3A.

25 The main difference between the Figure 2A and 2B and the Figure 3A and 3B
26 process conditions is the increased plasma source DC power (which was increased from

1 1 kW to 2 kW). Once again, the bottom coverage is significantly increased as process
2 chamber pressure is increased. It appears that sidewall coverage is also significantly
3 increased, although the data for sidewall coverage at the edge of the semiconductor
4 substrate, as illustrated by curve 328 is not conclusive. It may be that at higher chamber
5 pressures (above 40 mT), the data would be more conclusive for edge-of-wafer sidewall
6 coverage. However, the higher plasma source power leads to increased deposition rates
7 which result in inefficient ionization. For this particular equipment, lower source powers
8 in the range of about 1 kW are preferred.

9 Figure 4A shows a plot 400 of simulated ionization fraction (which can be
10 converted to per cent by multiplying by 100) as a function of the process chamber
11 pressure, all other variables held constant at the values specified with reference to
12 Figures 2A and 2 B. Ionization fraction is shown on vertical axis 402 and process
13 chamber pressure is shown on horizontal axis 404. Curve 406 represents data at the
14 center of the semiconductor wafer substrate, while curve 408 represents data at the edge
15 of the semiconductor wafer substrate. Figure 4 A illustrates that an increase in process
16 chamber pressure is helpful in increasing both the ionization fraction, and at higher
17 pressures (50 mT and higher) is also helpful in obtaining uniformity of ionization
18 fraction across the substrate surface.

19 Figure 4B shows a plot 420 of ionization fraction as a function of the power
20 applied to the ionization coil, all other variables held constant at the values specified with
21 reference to Figure 4A and at a process chamber pressure of 20 mT. Curve 426
22 represents data at the center of the semiconductor wafer substrate, while curve 428
23 represents data at the edge of the wafer substrate. Not only is the ionization fraction
24 lower than desired at the edge of the wafer substrate, but an increase in power to the
25 ionization coil does not provide a uniform ionized fraction across the substrate surface.

26 One skilled in the art can envision a number of possible semiconductor structures

1 where the present invention could be used to ensure a sufficient step coverage of the seed
2 layer to enable the complete filling of copper interconnect and contact features. Such
3 semiconductor structures may include the use of a dielectric substrate other than silicon
4 dioxide (such as a low k polymeric dielectric substrate); may include the use of barrier
5 layers other than tantalum nitride, such as tantalum, titanium, titanium nitride, tungsten,
6 tungsten nitride, or combinations thereof; may include a wetting layer of a material other
7 than copper (such as aluminum); and may include the use of a copper fill layer applied by
8 a techniques other than electrolytic plating. In addition, the high ionization fraction may
9 be obtained using apparatus known in the art, other than that described herein. The above
10 described preferred embodiments are not intended to limit the scope of the present
11 invention, as one skilled in the art can, in view of the present disclosure expand such
12 embodiments to correspond with the subject matter of the invention claimed below.

CLAIMS

We claim:

- 1 1. A method of providing a continuous copper seed layer upon or within semiconductor
2 substrate, said method comprising: depositing said copper seed layer over an interior
3 surface of said feature using copper species wherein at least 30 per cent of the species are
4 in the form of copper ions at the time said species contact said substrate surface.
- 1 2. The method of Claim 1, wherein said percent of species which are ions ranges
2 between about 50 % and about 100 %.
- 1 3. The method of Claim 2, wherein said percent of species which are ions ranges
2 between about 50 % and about 90 %.
- 1 4. The method of Claim 3, wherein said percent of species which are ions ranges
2 between about 60 % and about 90 %.
- 1 5. The method of Claim 1, or Claim 2, or Claim 3, or Claim 4, wherein said percentage
2 of copper species which are ions is obtained by applying power to an ionizing device
3 located between a source of said copper species and said semiconductor substrate, and
4 wherein the ambient pressure surrounding the copper species at the time of application of
5 the ionization energy provided by said RF power source is at least 30 mT.
- 1 6. The method of Claim 5, wherein said ambient pressure is at least 40 mT.
- 1 7. The method of Claim 6, wherein said ambient pressure is at least 60 mT.

- 1 8. An apparatus used to provide a continuous copper seed layer upon or within
2 semiconductor substrate, according to the method of Claim 1, said apparatus including
3 an electronic device which is programmed to carry out steps of said method.
- 1 9. The apparatus of Claim 8, wherein said apparatus also includes an ionizing device
2 located between a source used to generate copper species and said semiconductor
3 substrate.
- 1 10. The apparatus of Claim 9, wherein RF power is applied to said ionizing device.
- 1 11. A method of providing a complete copper fill of a semiconductor feature upon or
2 within semiconductor substrate, said method comprising: depositing a copper fill seed
3 layer over an interior surface of said feature using copper species wherein at least 30 per
4 cent of the species are in the form of copper ions at the time said species contact said
5 substrate surface.
- 1 12. The method of Claim 11, wherein said percent of species which are ions ranges
2 between about 30 % and about 90 %.
- 1 13. The method of Claim 12, wherein said percent of species which are ions ranges
2 between about 50 % and about 90 %.
- 1 14. The method of Claim 13, wherein said percent of species which are ions ranges
2 between about 70 % and about 90 %.

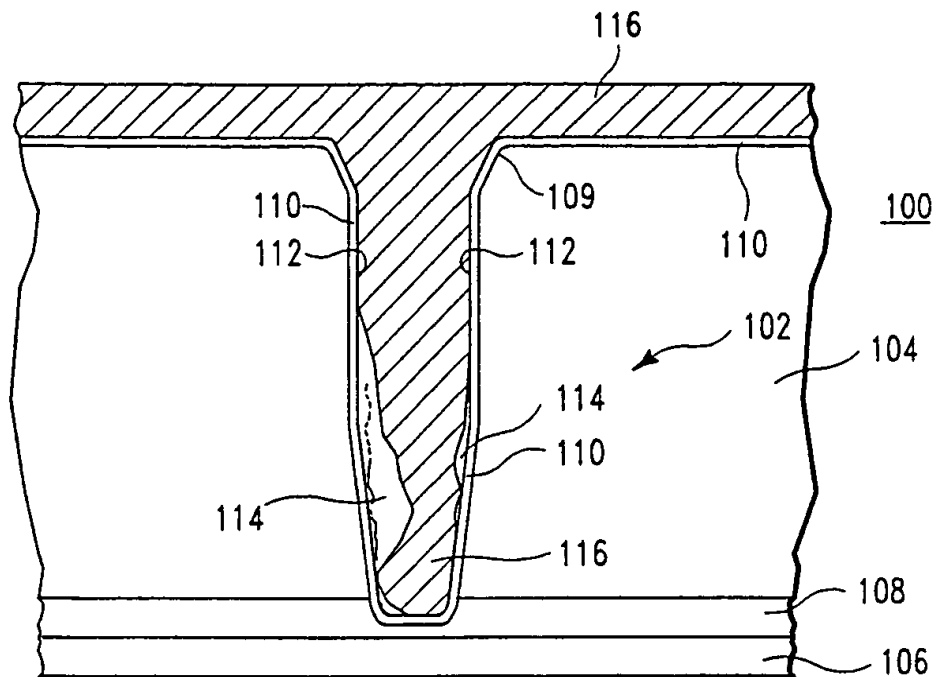
1 15. The method of Claim 11, or Claim 12, or Claim 13, or Claim 14, wherein said
2 percentage of copper species which are ions is obtained by applying power to an ionizing
3 device located between a source of said copper species and said semiconductor substrate,
4 and wherein the ambient pressure surrounding the copper species at the time of
5 application of the ionization energy provided by said RF power source is at least 30 mT.

1 16. An apparatus used to provide a complete copper fill of a semiconductor feature,
2 according to the method of Claim 11, said apparatus including an electronic device
3 which is programmed to carry out steps of said method.

1 17. The apparatus of Claim 16, wherein said apparatus also includes an ionizing device
2 located between a source used to generate copper species and said semiconductor
3 substrate.

1 18. The apparatus of Claim 17, wherein RF power is applied to said ionizing device.

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(PRIOR ART)

FIG. 1A

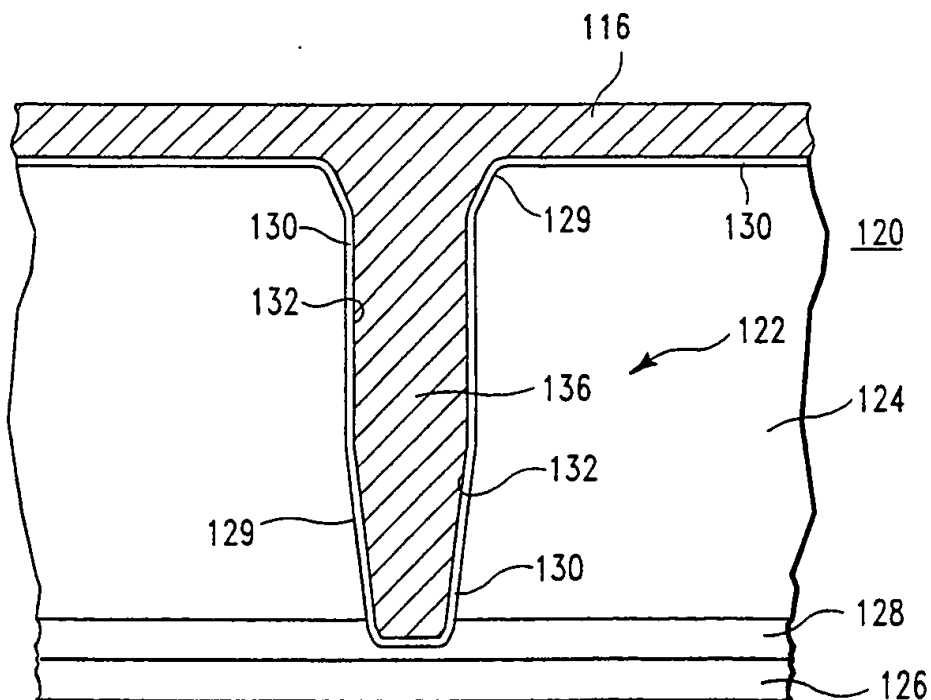


FIG. 1B

SUBSTITUTE SHEET (RULE 26)

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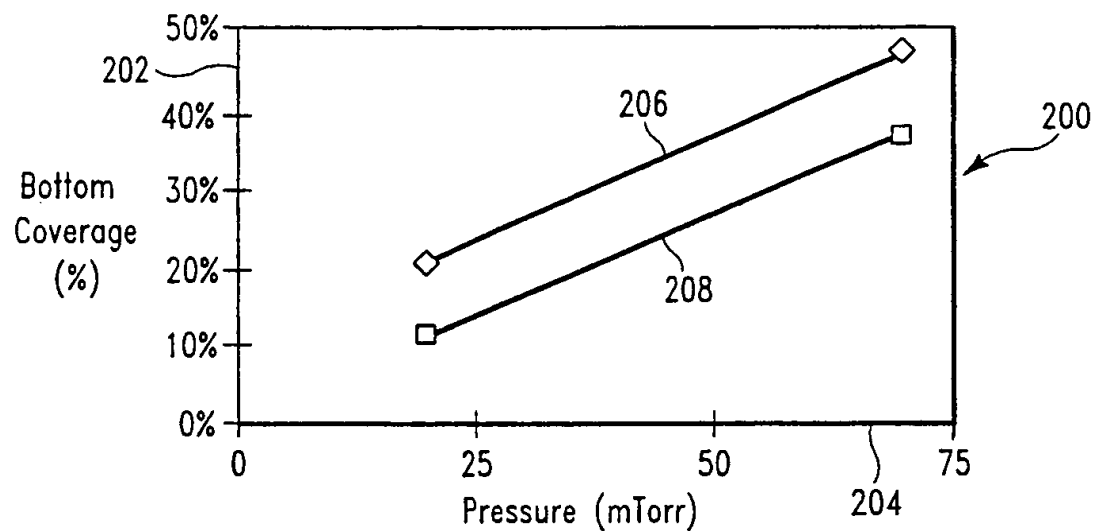


FIG. 2A

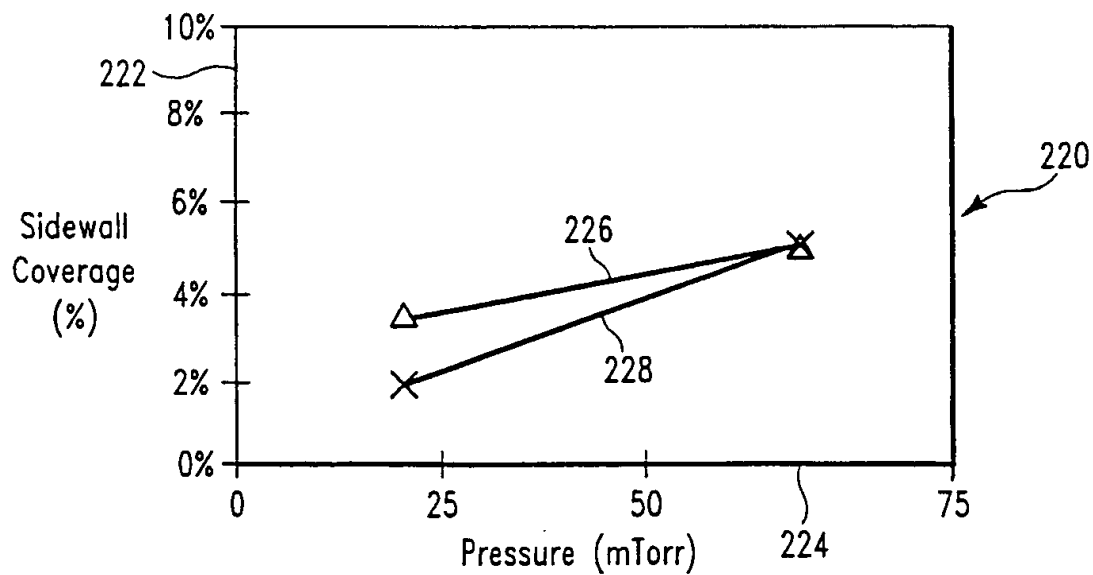


FIG. 2B

3 / 5

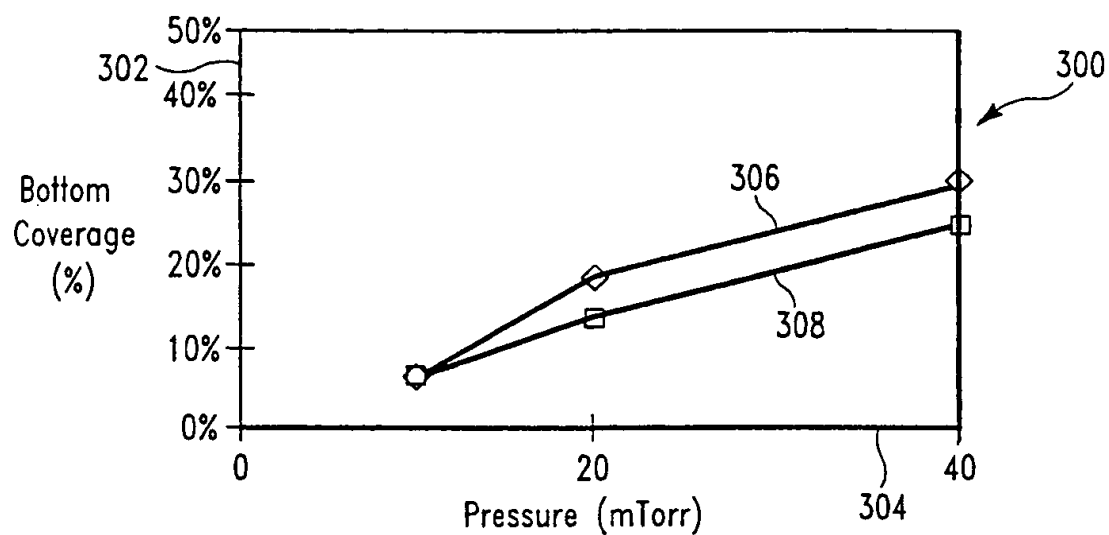


FIG. 3A

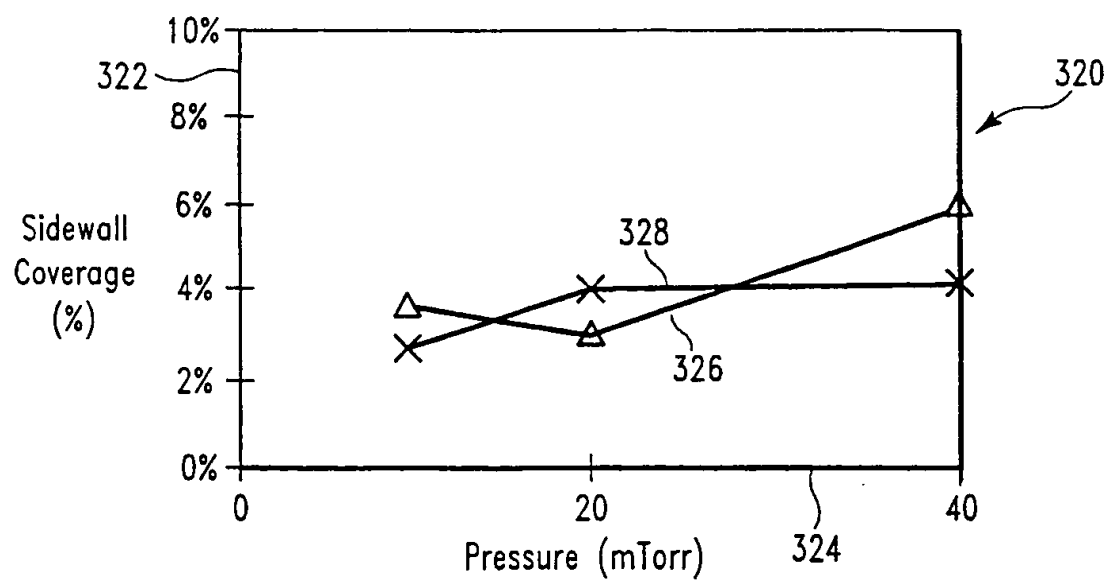


FIG. 3B

4 / 5

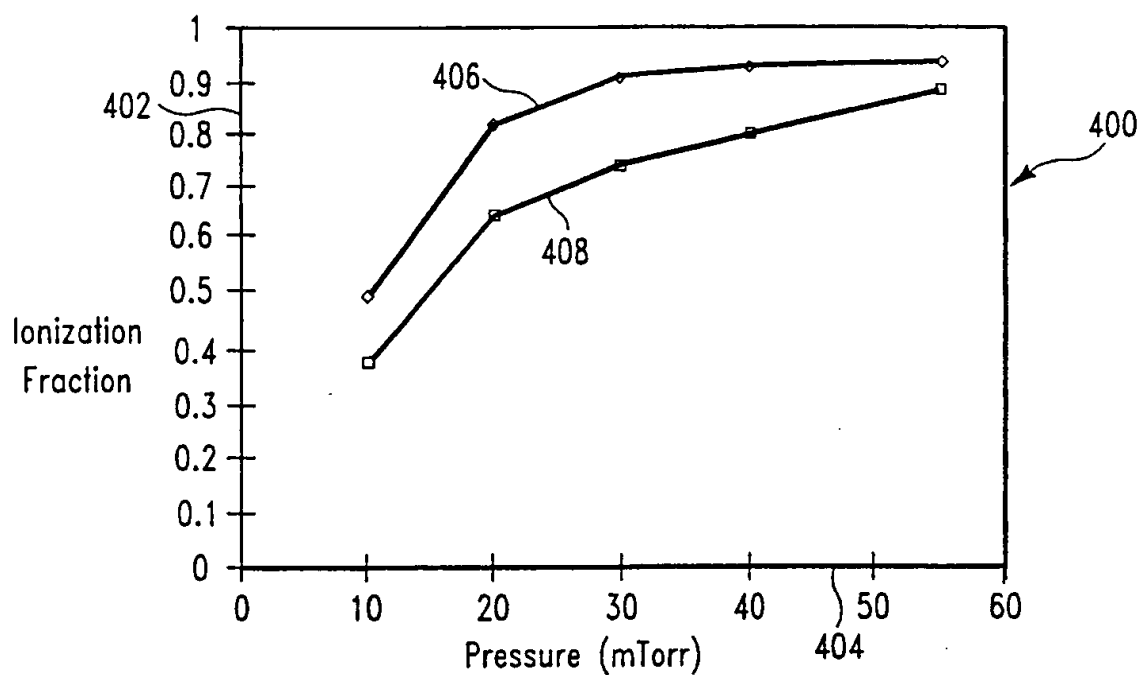


FIG. 4A

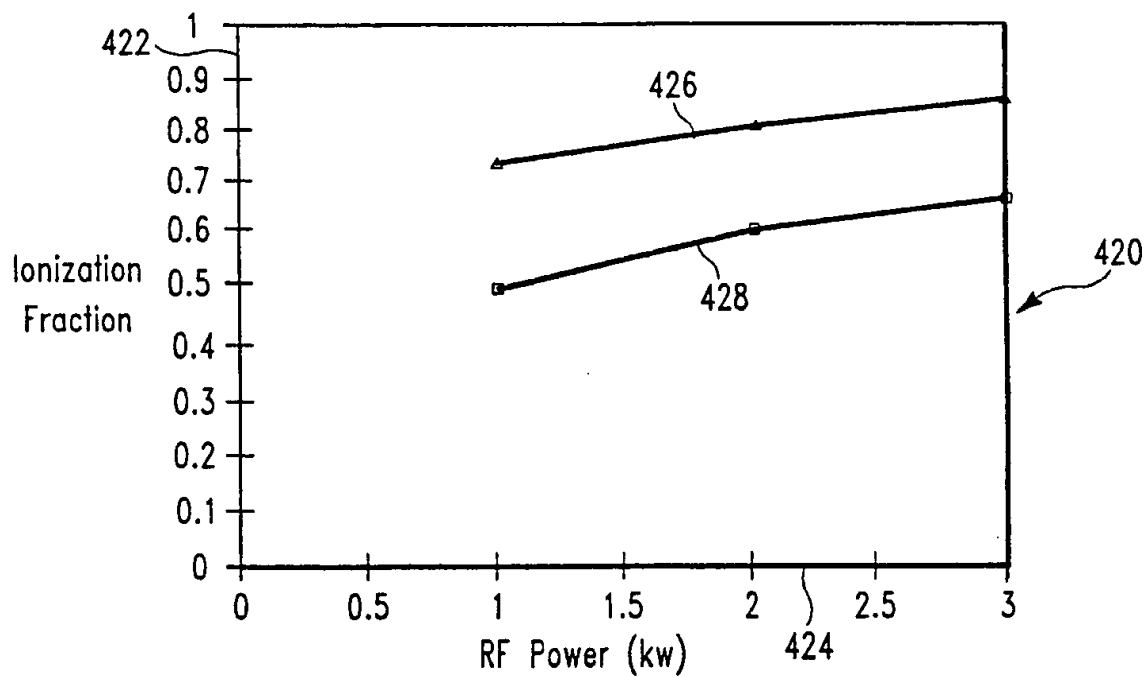
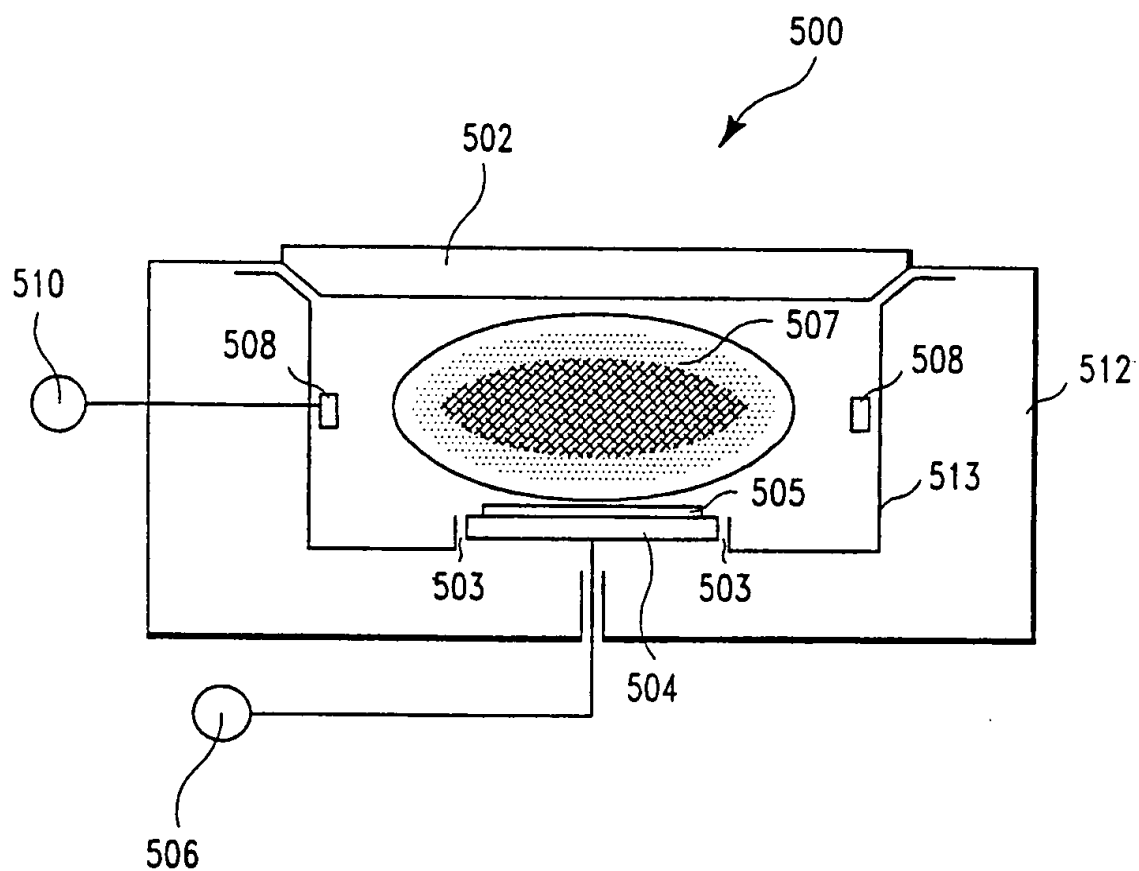


FIG. 4B



(PRIOR ART)

FIG. 5

INTERNATIONAL SEARCH REPORT

In Application No

PCT/US 99/30235

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768 H01L21/285

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 878 843 A (APPLIED MATERIALS INC) 18 November 1998 (1998-11-18) cited in the application column 9, line 10 - line 55 column 11, line 34 -column 12, line 4	1-7, 11-15
X A	EP 0 799 903 A (APPLIED MATERIALS INC) 8 October 1997 (1997-10-08) column 12, line 7 - line 22 column 13, line 2 -column 14, line 24 column 15, line 16 - line 19 column 17, line 1 -column 18, line 6; figure 10 -/-	8-10, 16-18 1-7, 11-15

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.*** Special categories of cited documents :*****A*** document defining the general state of the art which is not considered to be of particular relevance***E*** earlier document but published on or after the international filing date***L*** document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)***O*** document referring to an oral disclosure, use, exhibition or other means***P*** document published prior to the international filing date but later than the priority date claimed***T*** later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention***X*** document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone***Y*** document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.***Z*** document member of the same patent family

Date of the actual completion of the international search

16 May 2000

Date of mailing of the international search report

31.05.2000

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Micke, K

INTERNATIONAL SEARCH REPORT

Int. Application No
PCT/US 99/30235

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 98 59087 A (APPLIED MATERIALS INC ;APPLIED SCIENCE & TECHNOLOGY I (US)) 30 December 1998 (1998-12-30) page 4, line 22 -page 5, line 30 page 6, line 18 -page 10, line 26; figures 1,3A-F	1-4,8, 11-14,16
X	A.I.VLADIMIROV ET AL: "Metal-Plasma Source" INSTRUM.EXP.TECH., vol. 30, no. 2/2, March 1987 (1987-03), pages 395-398, XP000910344 USA the whole document	1
P,X	MONTEIRO O R: "Novel metallization technique for filling 100-nm-wide trenches and vias with very high aspect ratio" JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B (MICROELECTRONICS AND NANOMETER STRUCTURES), MAY-JUNE 1999, AIP FOR AMERICAN VACUUM SOC, USA, vol. 17, no. 3, pages 1094-1097, XP002137827 ISSN: 0734-211X the whole document	1-4, 11-14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 99/30235

Box I Observations where certain claims were found unsearchable (Continuation of Item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of Item 2 of first sheet)

This International Searching Authority found multiple inventions in this International application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US 99 /30235

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims 1-4,11-14:

The applicant has chosen to define the invention by its result, in that he claims a method but does not specify the process parameters necessary to perform the method (PCT Prel. Exam. Guidelines, Chapter III-4.7). On the other hand, the process parameters supported by the description (p.16) are covered by ep878843, cited by the applicant, and according to the description on p.16, these parameters should result in an ionization percentage of 80%, making ep878843 a novelty destroying document for all method claims.

The search was performed for a copper deposition method wherein the fraction of copper ions are in the claimed range, but the search may not be complete as to other process parameters/process features that may achieve this result.

Claims 8-10,16-18:

For these claims there is some doubt concerning the claim category, since an apparatus is claimed by its use (PCT Prel.Exam.Guidelines Chapter III-4.1 and 4.8a).

A deposition apparatus including a programmable electronic device and an RF powered ionizing device between the source material and the substrate was searched.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. App. No. Application No

PCT/US 99/30235

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0878843	A	18-11-1998	NONE	
EP 0799903	A	08-10-1997	JP 9120991 A US 6045666 A	06-05-1997 04-04-2000
WO 9859087	A	30-12-1998	EP 0996762 A	03-05-2000

Form PCT/ISA/210 (patent family annex) (July 1992)

